AMENDMENTS IN THE CLAIMS

1. (currently amended) A circuit for programming and testing electrical fuse (eFuse) circuits in a device, said circuit comprising:

an eFuse circuit that includes a fuse, a blow device, and a control input for said blow device;

first logic means for determining when to blow said fuse, wherein said first logic means comprises:

a first latch component having multiple inputs and which provides a true output;

a second latch component having multiple inputs and which provides both a second true output and a complement output;

wherein said second latch component is programmed with a blow value for said fuse such that the blow value dictates when a fuse is to be blown; and

an EFUSEPROGRAM signal that together with said true output and said second true output provides the control input to said blow device; [[and]]

second logic means for triggering a bypass of a pre-blow process within said eFuse circuit when said fuse is not to be blown, wherein a shifted 1 propagating through a plurality of eFuse circuits within said device is passed to a next downstream eFuse circuit without delay attributable to said pre-blow process; wherein said second logic means comprises:

an AND gate having a first input coupled to said complement output of said second latch, a second input coupled to said program signal, and a result output;

a multiplexer (MUX) having a first MUX input coupled to the true output of said first latch component, a second MUX input coupled to a selected output of a previous MUX of a third eFuse circuit sequentially before said eFuse circuit, a select input coupled to said result output of said AND gate, and a select output; and

third logic means for maintaining the EFUSEPROGRAM signal in a logic low state during serial readout of fuse latches within a shift path, such that the MUX is forced to choose the input from a fuse latch of the circuit and the fuse latch is forced to be within the shift path regardless of the state of the pattern latch.

2-4. (canceled)

5. (currently amended) The circuit of Claim [[4]] 1, wherein further:

said first MUX input is selected when said result output is low (0);

said second MUX input is selected when said result output is high (1); and

said blow device is triggered to blow said fuse when said first MUX input is selected and both said true output and said second true output are high.

6. (currently amended) In a device that includes multiple, serially connected, electrical fuse (eFuse) circuits, a system for programming and testing eFuse circuits, said system comprising:

an AND gate having two inputs and a result output;

a multiplexer (MUX) having a first input, a second input, a select input, and a MUX output, wherein select input is coupled to said result output of said AND gate;

wherein, said eFuse circuit includes a fuse coupled to a switch that is controlled by signals from a fuse latch, a pattern latch, and a program signal source, said pattern latch being programmed with a fuse blow status indicating whether or not said fuse is to be blown during device testing; [[and]]

first logic means for determining when to blow said fuse, wherein said first logic means comprises an EFUSEPROGRAM signal that together with said true output and said second true output provides the control input to said blow device;

second logic means for enabling a bypass of a pre-blow process within said eFuse circuit when said fuse blow status indicates that said fuse is not to be blown, such that a time delay associated with said fuse-blow process is substantially eliminated as a testing operation proceeds to each eFuse circuit within said device; and

third logic means for maintaining the EFUSEPROGRAM signal in a logic low state during serial readout of fuse latches within a shift path, such that the MUX is forced to choose the input from a fuse latch of the circuit and the fuse latch is forced to be within the shift path regardless of the state of the pattern latch.

7. (currently amended) The system of Claim 6, wherein said second logic means for enabling the bypass includes connecting components and signals of said eFuse circuit to said MUX and said AND gate, wherein said MUX and said AND gate provide a bypass function that determines when a shifted "1" that is being serially propagated to each of said eFuse circuits

should be forwarded to said fuse latch for initiating a blow of said fuse, wherein when a fuse blow status within said pattern latch indicates that said fuse is not to be blown, said MUX forwards said shifted 1 to a next eFuse circuit without waiting on a completion of said pre-blow process.

8. (original) The circuit of Claim 6, wherein:

a first input of said AND gate is coupled to a complement of a signal from said pattern latch indicating the fuse blow status;

a second input of said AND logic is coupled to said program signal source;

said first input of said MUX is coupled to said fuse latch; and

said second input of said MUX is coupled to a MUX output of a previous MUX.

9. (original) The system of Claim 8, wherein further said MUX output of said MUX is connected to a second input of a next MUX of a next eFuse circuit.

10. (currently amended) The system of Claim 7, wherein said second input of said MUX is coupled to a "fuse in" signal when said MUX is a first MUX in said serially connected eFuse circuits.

11. (original) The system of Claim 6, wherein, said eFuse circuit is a first eFuse circuit that is serially connected to a second eFuse circuit, whose fuse blow status indicates its fuse should not be blown, and a third eFuse circuit whose fuse blow status indicates its fuse should be blown, said circuit comprising:

means for first routing said shifted 1 through said fuse latch of said first eFuse circuit, subsequently bypassing a fuse latch of said second eFuse circuit, and then routing said shifted 1 through a fuse latch of said third eFuse circuit, wherein only said first eFuse circuit and said third eFuse circuit utilizes processing time for routing said shifted 1 through respective fuse latches before forwarding said shifted 1 to a next eFuse circuit.

12. (currently amended) In a device that includes multiple, serially connected eFuse circuits, each having a fuse, a fuse switch, a fuse latch, a pattern latch, a fuse program signal,

AND logic and a bypass multiplexer (MUX), a method for reducing programming and testing time for said device comprising:

storing a fuse blow status within said pattern latch;

ANDing a complement of said fuse blow status with said fuse program signal;

selecting one of two inputs of said MUX based on a result of said ANDing step, said inputs including a first input coupled to a true output of said fuse latch and a second input coupled to a MUX output of a previous eFuse circuit;

forwarding a shifted 1 propagating through said device to a next eFuse circuit without waiting for a pre-blow processing time to elapse when said second input is selected, wherein a time delay for propagating said shifted 1 through said eFuse circuit is substantially eliminated;

determining when to blow said fuse, wherein said first logic means comprises an EFUSEPROGRAM signal that together with said true output and said second true output provides the control input to said blow device; and

maintaining the EFUSEPROGRAM signal in a logic low state during serial readout of fuse latches within a shift path, such that the MUX is forced to choose the input from a fuse latch of the circuit and the fuse latch is forced to be within the shift path regardless of the state of the pattern latch.

13. (new) The circuit of Claim 1, wherein the pattern latch register controls an "effective length" of the fuse latch register to equal a number of logic high states (1) onset latches in the pattern register only when EFUSEPROGRAM is at a logic high state.

14. (new) The circuit of Claim 1, wherein a fuse blow process is indicated for an effuse circuit if the MUX selects the fuse latch input, and the fuse blow process is completed before the shifted 1 is passed to the next eFuse circuit.

15. (new) The circuit of Claim 1, wherein when the MUX does not select the fuse latch input, the MUX bypass input is selected and the shifted 1 is sent to the next eFuse circuit.

16. (new) The system of Claim 6, wherein the pattern latch register controls an "effective length" of the fuse latch register to equal a number of logic high states (1) onset latches in the pattern register only when EFUSEPROGRAM is at a logic high state.

17. (new) The system of Claim 6, wherein a fuse blow process is indicated for an effuse circuit if the MUX selects the fuse latch input, and the fuse blow process is completed before the shifted 1 is passed to the next eFuse circuit.

18. (new) The system of Claim 6, wherein when the MUX does not select the fuse latch input, the MUX bypass input is selected and the shifted 1 is sent to the next eFuse circuit.

19. (new) The method of Claim 12, further comprising controlling, via the pattern latch register, an "effective length" of the fuse latch register to equal a number of logic high states (1) onset latches in the pattern register only when EFUSEPROGRAM is at a logic high state.

20. (new) The method of Claim 12, further comprising:

indicating a fuse blow process for an eFuse circuit if the MUX selects the fuse latch input, and completing the fuse blow process before the shifted 1 is passed to the next eFuse circuit; and

selecting the MUX bypass input and forwarding the shifted 1 to the next eFuse circuit when the MUX does not select the fuse latch input.